REMARKS/ARGUMENTS

Claims 1-3, 5-7 and 9-14 are pending. Claims 13-14 have been amended. Reconsideration is respectfully requested.

1. Objections to Claims 13-14

Claims 13-14 are objected to for depending upon a cancelled claim. Claims 13-14 have been amended to depend from claim 1 to overcome this objection.

2. Rejection of Claims 1-3, 5-7 and 9-14 Under §103(a)

Claims 1-3, 5-7 and 9-14 stand rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent Publication 2001/0033278 (Ohta) in view of U.S. Patent 7,079,122 (Morita). The Applicant respectfully traverses this rejection.

Claim 1 recites a circuit arrangement for controlling a display that includes, among other things, a row drive circuit (which includes a shift register for driving n rows of the display device sequentially from 1 to n responsive to a row enable signal that is provided to each row from 1 to n), and a column drive circuit (for driving m columns of the display device by supplying column voltages to the m columns corresponding to picture data to be displayed as pixels of the controlled row). A logic function is included in the row drive circuit in front of row outputs, which is configured to respond to a first control signal having one or more pulses indicative of whether or not the partial mode is to be implemented, by preventing one or more of the row outputs from driving one or more of the rows in response to the row enable signal. The row drive circuit includes a shift register which has n stages and n outputs, and in that a second control signal can be supplied to the shift register at an input thereof for controlling the consecutive rows 1 to n, which second control signal activates the outputs of the shift register consecutively in dependence on pulses of a clock signal. The logic function is connected between the n outputs of the shift register and the n rows of the display, the logic function configured to prevent the n outputs of the shift register from driving any of the n rows of the

display responsive to and during the one or more pulses of the first control signal, ***"wherein a frequency of the pulses of the clock signal increases during the one or more pulses of the first control signal."***

Similarly, claim 9 recites a drive circuit for controlling n rows of a display device that is operable in a partial mode, where the row drive circuit includes, among other things, a logic function connected in front of each of n outputs of a shift register. The logic function is configured to deactivate the n outputs of the shift register in dependence on the partial mode ***responsive to and during*** one or more pulses of a first control signal by preventing the n outputs of the shift register from driving the n rows of the display device. The outputs of the shift register are activated consecutively in dependence on pulses of a clock signal, ***where the frequency of the pulses of the clock signal increases during the one or more pulses of the first control signal.***

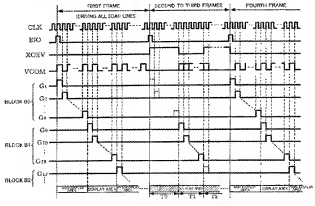
Claim 12 similarly recites sequentially providing an enable signal to enable each row in response to clock signal pulses, and deactivating row outputs during a first control signal first pulse, ***where the frequency of the clock signal pulses increases during the first control signal pulse***. The relationship between the increased frequency of the clock pulses during the (one or more) first control signal pulse(s) is illustrated in Fig. 3, and described on page 4, lines 7-31.

Ohta discloses a display device driving circuit that includes an output pulse control section 37b that deactivates the operation of the bi-direction shift register sections 33 through 36 in response to the GCNT2 signal (paragraph [0051]). However, as acknowledged by the Examiner on page 4 of the office action, Ohta does not disclose the frequency of the pulses of the clock signal increasing during the one or more pulses of the first control signal. Yet, the Examiner states that Morita discloses "the pulses of a clock signal (CLK) increases during the one or more pulses (i.e. one or more pulses in display are during time T1) of the first control signal (signal from logic section)" citing Fig. 11, column 14 (lines 45-67) and column 15 (lines 33-67), and that it would have been obvious "to incorporate the method of increasing the frequency of a clock signal during one or more pulses of the first control signal (signal from ligic

section) as taught by Morita in the scan driver of Ohta." The Applicant respectfully traverses this rejection on two grounds.

First, there is no apparent disclosure in Morita of increasing the frequency of the clock signal CLK, let alone doing so in response to a control signal. Fig. 12 of Morita shows that the frequency of the clock signal CLK is constant throughout the 1st through 4th frames (including through the non-display and display areas, and through all signals shown):

FIG. 12



Further, there is no apparent disclosure in column 14 (lines 45-67) and column 15 (lines 33-67) of Morita to increase the clock signal frequency. It is therefore not apparent why the Examiner concluded that the clock signal CLK increases in frequency during one or more pulses of the first control signal. If this rejection is maintained, clarification is respectfully requested.

Second, even if Morita disclosed increasing the frequency of the clock signal CLK during one or more pulses of a control signal (which the Applicant traverses), it is submitted it would not have been obvious to modify Ohta accordingly. Ohta specifically teaches decreasing the frequency of the clock signal for the non-display portions of the liquid crystal panel (see paragraphs [0065] and [0076]). The Applicant respectfully notes that it is improper to combine references where the references teach away from their combination. *In re Grasselli*, 713 F.2d 731, 218 USPQ 769, 779 (Fed. Cir. 1983); MPEP 2145(X)(D)(2). Ohta teaches away from a combination with another reference disclosing a clock frequency that is ***increased*** by specifically teaching that the clock rate should be ***decreased*** during a control signal signifying an area of the

display not to be scanned (see paragraph [0065] recited below). Moroever, a primary reference may not be modified in light of or combined with one or more secondary references where the result would be to render the primary reference inoperable for its intended purpose. *In re Gordon*, 733 F.2d 900, 902, 221 U.S.P.Q. 1125, 1127 (Fed. Cir. 1984). Modifying Ohta to increase the clock frequency instead of to decrease the clock frequency would render Ohta inoperable for the stated intended purpose of securing a sufficient quantity of charge for the pixels in the non-display portion (see paragraph [0065]).

> **[0065]** Here, the display data signals for the non-display portions **1***b* and **1***c* are used to charge the respective pixels by applying a voltage to the plurality of pixels with respect to a single data signal line. This might result in deficiency in amount of charge if the duration of voltage application is not different from normally, which, nonetheless, poses no serious problem since it occurs equally in all pixels and thus less color non-uniformity is caused on the non-display portions **1***b* and **1***c*. Nevertheless, in order to secure a sufficient quantity of charge for the pixels in the non-display portions **1***b* and **1***c*, the display data signals may be applied to the respective pixels longer than usual, for example, by increasing the cycle time of the source clock SCK for the control IC **4**, i.e., by decreasing the frequency, so as to increase the pulse width of the gate clock signal GCK.

Therefore, it is respectfully submitted that claims 1, 9 and 12 are not rendered unpatentable over Ohta in view of Morita because the combination of these two references does not appear to result in the claimed invention, and/or it would not have been obvious to modify Ohta as proposed by the Examiner. Claims 2-3, 5-7, 10-11 and 13-14 depend upon claim 1, 9 or 12, and are therefore considered allowable for the reasons set forth above.

For the foregoing reasons, it is respectfully submitted that the claims are in an allowable form, and action to that end is respectfully requested.

Respectfully submitted,

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